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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,317	01/23/2002	Guenter Knittel	10011617 -2	2879

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EXAMINER
LEHNER, WILLIAM P

ART UNIT	PAPER NUMBER
2671	5

DATE MAILED: 12/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.		Applicant(s)	
Office Action Summary	10/056,317		KNITTEL, GUENTER	
	Examiner		Art Unit	
	William P Lehner		2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-28* is/are allowed.

6)☒ Claim(s) *1-17 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2.   Claims 11 and 29-36 are rejected under 35 U.S.C. 112, second paragraph.

3.   Regarding claim 11, line 5, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

4.   Regarding claim 29 line 5, claims 30-32 line 2, and dependant claims, recite "an offline mechanism for storing the dataset in main memory..." does not make any sense. "Offline" means not connected to a computer or computer network. This is not referred to anywhere in the specification. So the claims are unclear as to exactly what these limitations are directed towards.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   Claims 1-3, 9, 10, and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lauer (6243098) in view of Kosaka (5163095).

3.   In regard to claim 1, An apparatus comprising a data set stored on machine-readable media, Note the data set of voxels stored on machine-readable DRAM or SRAM (column 8, lines 10-24) Wherein: the data set is divided into multiple subsets; The voxel data set is divided into blocked subsets (column 8, lines 49-58).

4.   A spread memory layout is implemented on the machine-readable media, the spread memory layout defining multiple pages in memory, Lauer does not have a spread memory layout and does not use pages.

Kosaka has a plurality of pages (column 7, line 65). Also, it is very conventional to

partition memory into pages for addressing.

5.   With a subset of data from the data set being mapped to one

or more predetermined portions of each page, Kosaka has an image data

set which is divided into multiple cells which are subsets (column 1, lines 10-17). Note

the subset image cells being mapped to predetermined addressable portions of the

page based on size (column 7, line 57 – column 8, line 34 and FIG 7). Each page has

cells (column 9, line 30).

6.   The portions being less than the capacity of each page; Note

the Kosaka's plurality of cells stored on a page (FIG 7).

7.   And each page is sized to map to quick access memory of a

processor, Kosaka has pages stored in image memories 22 and 24, and a

dedicated bus 18 transfers the mapped pages to the image processor 20 (FIG 1). Quick

random memory accessing is used to deliver data on a dedicated bus sixty times a

second (column 1, lines 37-49). Kosaka does not explicitly state that it sizes the page to

quickly map to the processor. DRAM is quick access memory. A burst of consecutive memory moving into or out of a quick access memory is known as a page. Lauer teaches that bursts of consecutive memory can be sized to a DRAM device's minimum burst size because this allows the processor to quickly fetch large amounts of data (column 9, lines 32-42).

8. Such that image data when fetched from the machine-readable media are mapped into one or more predetermined portions of quick access memory. Kosaka's cells are extracted to a designated address of the page (column 8, lines 23-34 and FIG 7).

9. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lauer to use pages to move data into quick access memory, to map the subsets to predetermined portions of the pages, and to set the page size for quick accesses by a processor as taught by Kosaka because this allows large amounts of data to be fetched quickly (see column 9, lines 35-58 of Kosaka). Also, the process of creating pages in memory is a conventional process in the setting up of memory address structure.

10. In regard to claim 2, Wherein the data set is primarily volumetric data, Note Lauer's volumetric voxel based data (column 1, lines 10-14). And wherein each subset is selected to be a cubic region of volumetric data, with all cubic regions being of like-size. Lauer has mini-block subsets, which are all the same size (column 9, lines 11-19).

11.   In regard to claim 3, Wherein each cubic region includes an 8x8x8 cube of voxels. Note Lauer's cube of voxels which could be 8x8x8 if the practical value of 8 is chosen for the variable B (column 9, lines 54-62).

12.   In regard to claim 9, wherein each subset occupies a specific contiguous location within each page Kosaka's subsets occupy specific contiguous locations within each page (FIG 7). That is at least one kilobyte in size. Lauer's subset blocks are sized to 8^3 or 512 voxels (column 32, line 8). Voxels are 16 bits each, or 2 bytes. 512 * 2 = 1024 bytes, or 1 kilobyte.

13.   In regard to claim 10, wherein each page is at least four kilobytes in size. Lauer can fit 4^3 or 64 subsets in a page burst (column 20, lines 21-33 and FIG 11). Lauer's subset blocks are sized to 8^3 or 512 voxels (column 32, line 8). Voxels are 16 bits each, or 2 bytes. 512 * 2 = 1024 bytes, or 1 kilobyte. At 1 kilobyte for every subset, the page burst size is 64 kilobytes.

14.   In regard to claims 12-14, wherein the image data is volumetric data and for each subset is stored on the machine-readable media in a cubically interleaved manner. Adjacent voxels are shaded alike in figure 11 are stored in the same page burst. They are cubic and occupy all three dimensions (column 20, lines 21-33 and FIG 11 of Lauer).

15.   Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Lauer (6243098) in view of Kosaka (5163095), in further view of Luick (6473835).

16.   In regard to claim 4, Wherein adapted for use where the quick

access memory is an on-chip processor cache, Lauer and Kosaka do not

say that his DRAM/SRAM device is a cache or that they are on the same chip as the

processor. Luick teaches that a cache may be used to store blocks of data that can be

more quickly accessed (column 1, lines 61-66). Therefore, it would have been obvious

to one of ordinary skill in the art at the time the invention was made to modify Lauer and

Kosaka to use a cache as taught by Luick because it allows data to be accessed faster.

17.   Luick teaches that a cache implemented on the same chip as a processor is

faster (column 3, lines 37-43). Therefore, it would have been obvious to one of ordinary

skill in the art at the time the invention was made to modify Lauer and Kosaka to have

cache on the same chip as the processor as taught by Luick because it is faster and

allows data that is often accessed to be quickly accessed and used.

18.   Wherein said apparatus further being characterized in that

the size of each page having any data from the data set

corresponds to size of the on-chip processor cache. The size of the

pages are the minimum burst size of the cache (see Lauer column 9, lines 32-42).

19.   In regard to claim 5, Adapted for use where the quick access

memory is a processor cache, Lauer's DRAM/SRAM is modified by Luick to be

a processor cache (note the above rejection to claim 4). Said apparatus further

being characterized in that the size of each page having any data
from the data set is selected to map to at least a portion of the
processor cache. Page size is determined by the minimum burst size of the DRAM
(see Lauer column 9, lines 32-42).

20.   In regard to claim 6, wherein said apparatus is adapted for use
with a n-way associative cache, Lauer describes four DRAM devices
(column 8, lines 22-24) modified by Lam to be caches. Lauer and Kosaka do not use an
n-way associative cache. Luick uses an n-way associative cache (abstract) because it is
decreases the size of the translation look-aside buffer, (column 2, lines 59-65).
Therefore, it would have been obvious to one of ordinary skill in the art at the time the
invention was made to modify Lauer, Kosaka, and Lam to use an n-way associative
cache as taught by Luick because it decreases the size of the translation look-aside
buffer.

21.   Said apparatus being further characterized in that size of
each page having image data equals the size of the processor
cache divided by n. If the size of Luick's cache is 128 bytes and n is 16, then the
size of each page is 8 bytes (column 6, lines 62-64). 128 divided by 16 = 8.

22.   In regard to claim 7, further comprising sizing each page such
that a subset of data from the data set stored in that page
occupies less than one-half of page size, Lauer can fit 4^3 or 64 subsets
in a page burst (column 20, lines 21-33 and FIG 11). 1/64 is less than one half. And
such that data when fetched from machine-readable media can only

be loaded into predetermined lines of processor cache, Kosaka

modifies Lauer to load data into predetermined lines of the cache (column 7, line 57 –

column 8, line 34 and FIG 7). No more than one-half of processor cache

capacity. 1/64 is less than one half.

23. In regard to claim 8, wherein each page is sized such that a

subset of data from the data set stored in that page occupies no

more than approximately one-quarter of page size, Lauer can fit 4^3 or

64 subsets in a page burst (column 20, lines 21-33 and FIG 11). 1/64 is less than one

quarter. And wherein each subset occupies one or more

predetermined, consistent locations within a page, Kosaka modifies

Lauer to store subsets into addressable, predetermined, consistent locations within a

page (FIG 7). Such that all subsets of data from the data set are

mapped to one or more specific locations in processor cache each

time a page is retrieved from the machine-readable media. Kosaka's

subsets are mapped to specific locations (FIG 7) to be retrieved by the machine

readable media.

24. Claims 11, 29-32, 35, and 36 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Lauer (6243098) in view of Kosaka (5163095), in further view of

Fiacco (5860149)

25.   In regard to claim 11, adapted for use where the data set

substantially consists of image data, Lauer's voxels are image data

(column 1, line 12). Further comprising processing parameters selected

from the group of buffers, tables, a tile buffer, shading tables,

and rendering parameters, Lauer has processing elements (column 17, line 49),

and interpolation, storage, shader, and compositioning units column 18, lines 21-31),

buffers (column 24, lines 33-38), and tile buffer or interpolation unit (column 26, lines

10-19).

26.   The processing parameters being stored in a page of memory

at a location other than the one or more predetermined portions,

such as to inhibit overwrite of processing parameters by image

data. Lauer has image data but does not have these processing parameters on

different portions of a page from the image data. Fiacco teaches that header buffers

may be partitioned from the payload data (column 4, lines 43-49 and FIG 5) because

this is faster (column 1, lines 24-33). The blocks containing buffers and data may be

separately addressed (column 4, lines 38-41). Because the buffers and data are in

separate address locations, overwriting is inhibited. Therefore, it would have been

obvious to one of ordinary skill in the art at the time the invention was made to modify

Lauer and Kosaka to store the processing parameters and image data at separate

locations in the page as taught by Fiacco because it is faster and to help ensure the

integrity of both th data and the processing parameters.

27.   In regard to claim 29, An apparatus, comprising: a processor; a

quick access memory adapted for use by the processor in

processing a data set; Lauer has quick access DRAM (column 8, lines 24-28)

which is adapted to fetch voxels for a processor (column 15, lines 46-49). An offline

mechanism for storing the data set in a main memory using a

spread memory layout, wherein the spread memory layout is chosen

such that the data set is divided into subsets of data, the

subsets are each stored in a page of memory of predetermined

size, Kosaka modifies Lauer to have a spread memory layout with subsets of

predetermined size stored at predetermined addresses (column 7, line 57 column 8,

line 34 and FIG 7). The page size chosen to map to at least a

predetermined portion of the quick access memory, and the subsets

are restricted to occupy only a selected portion of each page;

Lauer's burst size is chosen off of the DRAM device's minimum burst size (column 9,

lines 32-42). Kosaka modifies Lauer to map subsets exclusively to predetermined

portions (FIG 7).

28.   And instructions stored on machine readable media that cause said processor to

load processing parameters used for processing the data set into the predetermined

portions of quick access memory; Lauer has processing elements (column 17, line 49).

Fiacco modifies Lauer to load processing parameters at predetermined portions of the

quick access memory (FIG 5). Wherein the selected portion of each page is chosen

such that the subsets of data will only occupy specific memory locations within mapped

portion of quick access memory, and wherein the instructions cause the loading of

processing parameters into the mapped portion of quick access memory at locations

other than the specific memory locations, such that the data set is inhibited from

overwriting processing parameters when data from the data set is retrieved from main

memory and loaded in mapped fashion into the quick access memory. Lauer does not

have these processing parameters on different portions of a page from the specific

image data. Fiacco teaches that header buffers may be partitioned from the payload

data (column 4, lines 43-49 and FIG 5) because this is faster (column 1, lines 24-33).

The blocks containing buffers and data may be separately addressed (column 4, lines

38-41). Because the buffers and data are in separate address locations, overwriting is

inhibited. Therefore, it would have been obvious to one of ordinary skill in the art at the

time the invention was made to modify Lauer and Kosaka to store the processing

parameters and specific image data at separate locations in the page as taught by

Fiacco because it is faster.

29.   In regard to claim 30-32, wherein the data set substantially

consists of image data and wherein the offline mechanism further

stores image data from the data set in a dimensionally-

interleaved manner, Such that each page in memory includes data

that is dimensionally-interleaved in two or more dimensions.

Voxels are image data (see Lauer column 1, line 12). Adjacent voxels are shaded alike

in figure 11 are stored in the same page burst. They are cubic and occupy all three

dimensions (see Lauer column 20, lines 21-33 and FIG 11). Also, Fiacco shows the

interleaving of data (FIG 5).

30.   In regard to claim 35, wherein the data set substantially consists

of volumetric data, said apparatus further comprising

instructions stored on machine-readable media that when executed

cause said processor to perform ray-casting using the data set.

Voxels are used in ray-casting (see Lauer column 14, lines 61-65).

31.   In regard to claim 36, wherein the processing parameters include

parameters selected from the group of a tile buffer, a pixel

buffer, shading coefficients, lighting coefficients, texture

information and light source information. Note Lauer's pixel buffer

(column 22, lines 63-64), light source information (column 4, line 23), lighting

coefficients (column 13, lines 66-67), shadow information (column 23, lines 26-34), tile

buffer or interpolation unit (column 26, lines 10-19) and texture information (column 3,

line 26).

32.   Claims 15, 16, 33, and 34 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Lauer (6243098) in view of Kosaka (5163095), in further view of

Luick (6473835), in further view of Fiacco (5860149).

33.   In regard to claim 15, An apparatus for processing a data set,

comprising: means for mapping data from the data set as part of a

page to one or more predetermined portions of a cache; Kosaka

modifies Lauer to map a dataset as part of a page (FIG 7). Luick modifies Lauer to map

pages to portions of the associative cache predetermined by the translation look-aside

buffer (column 2, lines 59-65).

34.   And means for mapping processing parameters as part of a
page to predetermined portions of the cache, such that processing
parameters occupy different portions of cache than data from the
data set; wherein the addressing of data from the data set and
processing parameters is thereby structured such that processing
parameters do not overwrite data from the data set when loaded
into the cache and such that data from the data set does not
overwrite processing parameters when loaded into the same cache.
Lauer has image data but does not have these processing parameters on different

portions of a page from the image data. Fiacco teaches that header buffers may be

partitioned from the payload data (column 4, lines 43-39) because this is faster (column

1, lines 24-33). The blocks containing buffers and data may be separately addressed

(column 4, lines 38-41). Because the buffers and data are in separate address

locations, overwriting is inhibited. Therefore, it would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Lauer and Kosaka

to store the processing parameters and image data at separate locations in the page as

taught by Fiacco because it is faster.

35.   In regard to claim 16, An apparatus according to claim 15, further
comprising: means for dimensionally-interleaving data from the
data set as discrete, contiguous subsets of data, such that each
subset represents a multidimensional space. Lauer dimensionally

interleaves voxels (column 16, lines 9-29 and FIG 4). Voxels represent 3D space (column 1, line 19). Subset blocks are discrete and contiguous (column 9, lines 54-62).

In regard to claim 33 , wherein the quick access memory is a n-way processor cache and wherein page size is selected to map the subsets to a predetermined portion of any of n sections of processor cache.

36.   In regard to claim 34, wherein the quick access memory is an on-chip processor cache.

37.   Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lauer (6243098) in view of Kosaka (5163095), in further view of Luick (6473835), in further view of Fiacco (5860149), in further view of Prevost (512384).

38.   In regard to claim 17, An apparatus according to claim 15, adapted for processing volumetric data, said apparatus further comprising: means for cubically-interleaving volumetric data representing three dimensions Lauer cubically interleaves voxels (column 16, lines 9-29 and FIG 4). Using oct-tree addressing. Lauer does not use octree addressing. Prevost uses octree addressing (column 20, line 32 and column 1, lines 40-50) because it is very fast (column 1, line 36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lauer to use octree addressing as taught by Prevost because it is fast and will improve the performance of the system.
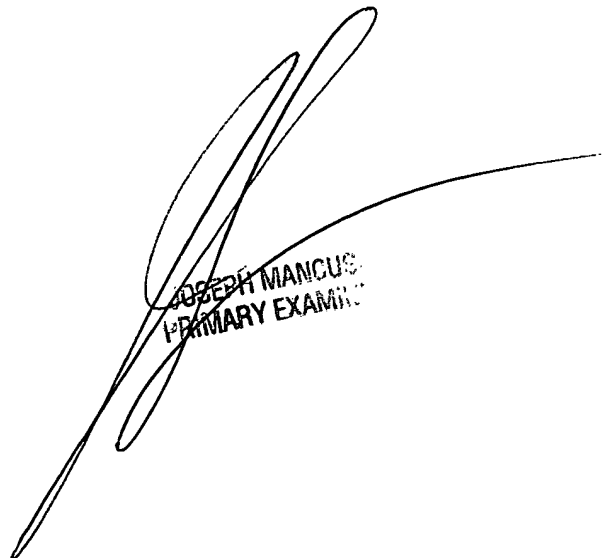
Allowable Subject Matter

39.   Claims 18-28 are allowed. Claim 18 claims a predetermined gap in the memory address between multiple subsets of the data. This limitation has not been found in the prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William P Lehner whose telephone number is 703-305-0682. The examiner can normally be reached on 8:30 - 5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman can be reached on 703-305-9798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

WPL

JOSEPH MANCUS
PRIMARY EXAMINER